Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-12 (Canceled)

13. (Allowed) A method for facilitating high signal throughput of an improved CMOS image sensor comprising a plurality of photo sensors configured in a two-dimensional area, [[;]] said method comprising:

reading out charge signals from said plurality of photo sensors row by row in parallel to respective column buses; said column buses coupled to a double sampling circuit and a programmable gain amplifier;

conditioning said charge signals in said programmable gain amplifier in accordance with said double sampling circuit before said charge signals are digitized to produce pixel signals; and

processing said pixel signals in a pixel processor to produce a desired result.

14. (Allowed) The method as recited in claim 13 wherein said pixel processor, said double sampling circuit and said programmable gain amplifier are monolithically integrated with said plurality of photo sensors of the CMOS image sensor.

15. (Allowed) The method as recited in claim 13 wherein said conditioning said charge signals comprises:

deriving a measurement difference of each of said charge signals with a reference in said double sampling circuit; and

adjusting said each of said charge signals with respect to said measurement difference said programmable gain amplifier.

16. (Allowed) The method as recited in claim 13 wherein said desired result is a compressed format of said pixel signals and wherein said processing said pixel signals in a pixel processor comprises compressing said pixel signals according to a commonly used compression standard.

17. (Allowed) The method as recited in claim 16 wherein the commonly used compression standard is selected from a group consisting of Graphic Interchange Format (GIF), JPEG (Joint Photographic Experts Group) and MPEG (Moving Picture Experts Group) supported by a World Wide Web protocol.

18. (Allowed) The method as recited in claim 13 wherein said desired result is a gray-scale intensity image and wherein said processing said pixel signals in a pixel processor comprises converting said pixel signals respectively to intensity data according to a predefined conversion standard.

19. (Currently Amended) An architecture for facilitating high signal throughput of an improved CMOS image sensor comprising a plurality of photo sensors configured in a two-dimensional area,[[;]] said architecture comprising:

a pair of column address and row address decoders providing address signals to address each of the plurality of photo sensors;

a number of signal conditioning circuits, ~~each~~ said signal conditioning circuits comprising a correlated double sampling circuit and a programmable gain amplifier, said signal conditioning circuits coupled to a column data bus for receiving charge signals ~~readout~~ read out from said photo sensors when said photo sensors are addressed by said address signals;

a number of analog-to-digital converters, each respectively coupled to one of said conditioning circuits and digitizing said charge signals in parallel[[;]] to produce pixel signals; and

a pixel processor for receiving said pixel signals from said analog-to-digital converters, wherein said pixel signals are processed to produce a desired result[[,]] .

20. (Canceled)

21. (Currently Amended) The architecture as recited in claim 19 [[20]]wherein said correlated double sampling circuit derives a measurement difference of each of said charge signals with a reference.

22. (Currently Amended) The architecture as recited in claim 21 wherein said ~~programmer~~ programmable gain amplifier receives said measurement difference and adjusts said each of said charge signals with respect to said measurement difference.

23. (Original) The architecture as recited in claim 21 wherein each of the signal conditioning circuits produces a signal that indicates an optimum exposure time.

24. (Currently Amended) The architecture as recited in claim 23 wherein said correlated double sampling circuit and said ~~programmer~~ programmable gain amplifier together ~~derives~~ derive a measurement difference of each of said charge signals with a reference; and ~~calculates~~ calculate said optimum exposure time from said measurement difference.

25. (Currently Amended) The architecture as recited in claim 19 [[20]]further comprises a memory storing instructions[[;]]said memory coupled to said pixel processor that executes said instructions from said memory to achieve said desired result.

26. (Currently Amended) The architecture as recited in claim 25 wherein said instructions ~~causes~~ cause said pixel processor to compress said pixel signals according to a commonly used compression standard.

27. (Currently Amended) The architecture as recited in claim 26 wherein the commonly used compression standard is selected from a group consisting of GIF (Graphic Interchange Format) ~~(GIF)~~, JPEG (Joint Photographic Experts Group) and MPEG (Moving Picture Experts Group) supported by a World Wide Web protocol.

28. (Currently Amended) The architecture as recited in claim 25 wherein said instructions ~~causes~~ cause said pixel processor to convert said pixel signals respectively to intensity data according to a predefined conversion standard.

29. (Currently Amended) The architecture as recited in claim 19 wherein said pixel processor is monolithically integrated with said plurality of photo sensors.

30. (Currently Amended) The architecture as recited in claim 19 [[20]] wherein said pixel processor, said correlated double sampling circuit and said ~~programmer~~ programmable gain amplifier are [[is]] monolithically integrated with said plurality of photo sensors.

31. (New) An architecture for facilitating high signal throughput of an improved CMOS image sensor comprising a plurality of photo sensors configured in a two-dimensional area; said architecture comprising:

a pair of column address and row address decoders providing address signals to address each of the plurality of photo sensors;

a number of signal conditioning circuits, each coupled to a column data bus for receiving charge signals read out from said photo sensors when said photo sensors are addressed by said address signals;

a number of analog-to-digital converters, each respectively coupled to one of said conditioning circuits and digitizing said charge signals in parallel to produce pixel signals;

a pixel processor for receiving said pixel signals from said analog-to-digital converters;

a memory loaded with one or more instructions accessed by the pixel processor; and

wherein said pixel signals are processed to produce a desired result.

32. (New) The architecture as recited in claim 31 wherein each of the signal conditioning circuits comprises a correlated doubled sampling circuit and a programmable gain amplifier.

33. (New) The architecture as recited in claim 32 wherein said correlated double sampling circuit derives a measurement difference of each of said charge signals with a reference.

34. (New) The architecture as recited in claim 33 wherein said programmable gain amplifier receives said measurement difference and adjusts said each of said charge signals with respect to said measurement difference.

35. (New) The architecture as recited in claim 33 wherein each of the signal conditioning circuits produces a signal that indicates an optimum exposure time.

36. (New) The architecture as recited in claim 35 wherein said correlated double sampling circuit and said programmable gain amplifier together derive a measurement difference of each of said charge signals with a reference; and calculate said optimum exposure time from said measurement difference.

37. (New) The architecture as recited in claim 31 wherein said instructions cause said pixel processor to compress said pixel signals according to a commonly used compression standard.

38. (New) The architecture as recited in claim 37 wherein the commonly used compression standard is selected from a group consisting of GIF (Graphic Interchange Format), JPEG (Joint Photographic Experts Group) and MPEG (Moving Picture Experts Group) supported by a World Wide Web protocol.

39. (New) The architecture as recited in claim 31 wherein said instructions cause said pixel processor to convert said pixel signals respectively to intensity data according to a predefined conversion standard.

40. (New) The architecture as recited in claim 31 wherein said pixel processor is monolithically integrated with said plurality of photo sensors.

41. (New) The architecture as recited in claim 32 wherein said pixel processor, said correlated double sampling circuit and said programmable gain amplifier are monolithically integrated with said plurality of photo sensors.